1. 연구실(실험실): Circuits & Systems Lab [http://cas.kau.ac.kr]

2. 담당 교수

성 명	전공분야	연락처	메일주소
김태환	Digital Circuits & Systems	02-300-0140	taehwan.kim@kau.kr

3. 연구 분야

-
  - Acceleration of Neural Network Inference & Training
  - Architecture-Aware Neural Network Model Design
  - Fault-Tolerant Neural Network Inference
-
  - Error-Correcting CODEC Processors
  - Detection & Decoding for Next-Generation MIMO System
  - Sound Synthesis Processor
  - Optical Distortion Correction Processor, Low-Complexity De-Weathering Systems
-

4. 연구원 모집 인원

- 대학원생 (MS or Ph.D Course): 2명
- 학부생: 4명
- Financial support (MS ≤ 2.5M) + TA/RA scholarship (대학원생)

5. 연구실 특장점

- 세계 최고 수준의 연구 지향 (Digital Circuits and Systems 분야)
- 학부 및 대학원 생 차별 없이 연구 지도 (본인 능력에 따른 역할 부여)

6. 최근 졸업생 취업현황

- [반도체 칩 설계 / 디자인 하우스] LIG Nex1, 오픈엣지, LX 세미콘, Synopsys, 삼성전자, 현대 모비스 등
- [유학] Georgia Inst. Tech., Univ. Texas at Austin 등

5. 최근 주요 논문

117 Research Papers and 43 Patents *(As of Oct. 2026 Since 2008) Including:*

- T.-H. Kim et al., "Softme^x: Lightweight Softmax Compute Engines Based on Exponentiation Units," [IEEE Trans. CAD 2026]
- J. Lee et al., "MiniBRNN: A Low-Resource Inference Processor for Binary-Weight Recurrent Neural Networks Based on Speculative Operation Pruning and Interleaved Thread Scheduling" [IEEE Trans. CAD 2025]
- J. Kim et al., "StabiFreeze: Early Stopping for Training Binary Neural Networks via Internal Dynamics Stabilization" [ASP-DAC 2026]
- G.-H.. Kwak et al., "SR-BIP: A Soft Error-Resilient Binary Neural Network Inference Processor" [IEEE Trans. CAD 2025]

■ G.-H.. Kwak et al., “BiNPU: A 33.0 MOP/s/LUT Binary Neural Network Inference Processor Showing 88.26% CIFAR10 Accuracy with 1.9 Mbit On-Chip Parameters in a 28 nm FPGA” [IEEE Trans. CAS-II 2024]
■ J. Kim et al., “ROSETTA: A Resource and Energy-Efficient Inference Processor for Recurrent Neural Networks Based on Programmable Data Formats and Dynamic Activation Pruning” [IEEE Trans. Emerging Topics in Computing 2023]
■ J. Kim et al., “A Reconfigurable Inference Processor for Recurrent Neural Networks Based on Programmable Data Format in a Resource-Limited FPGA” [ASP-DAC 2022]
■ T. Kim et al., “A resource-efficient inference accelerator for binary convolutional neural networks in a low-cost FPGA,” [IEEE Trans. CAS-I 2021]
■ H.-Y. Yoon et al., “A 655Mbps Successive-Cancellation Decoder for a 1024-Bit Polar Code in 180nm CMOS,” [ASSCC 2018]
■ Y.-M. Park et al., “Fast Execution of Dark-Channel-Prior-Based Outdoor Video Dehazing,” [IEEE ACCESS 2018]
■ H.-Y. Yoon et al., “Efficient Successive-Cancellation Polar Decoder Based on Redundant LLR Representation,” [IEEE Trans. CAS-II 2018]

7. 수상내역

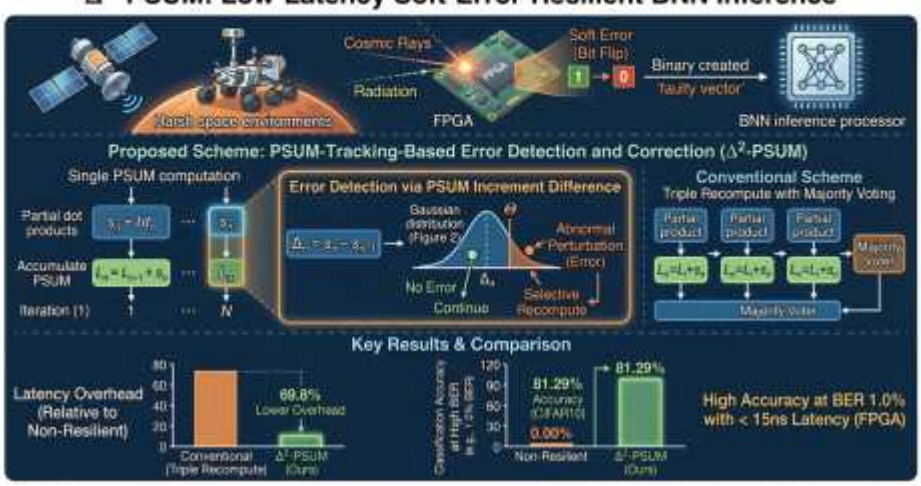


8. 연구내용 상세소개





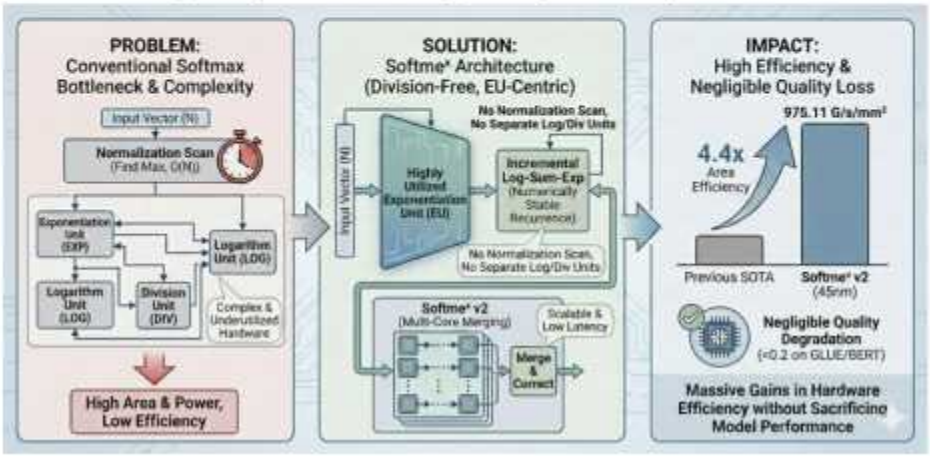
FCCM26





TCAD26

Softme^{x}: Lightweight Softmax Compute Engines via Exponentiation Units





TCAD26

MiniBRNN: A Low-Resource Inference Processor for Binary-Weight Recurrent Neural Networks Based on Speculative Operation Pruning and Interleaved Thread Scheduling

